

LIST OF PRIOR ART CITED BY  
APPLICANT

(PTO-1449)

ATTY. DOCKET NO.  
INTEL-0065APPLN. SERIAL NO.  
New U.S. Patent  
Application 10/813,084APPLICANT(S)  
Maged M. GHONEIMA et alFILING DATE  
March 31, 2004GROUP 2819  
~~To be assigned~~

## U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	*PATENT NO.	*ISSUE DATE	*INVENTOR NAME	CLASS	SUBCLASS	FILING DATE

## U.S. PATENT APPLICATION PUBLICATIONS

	*PATENT APPLN. PUB. NO.	*PUB. DATE	*APPLICANT	CLASS	SUBCLASS	

## U.S. PATENT APPLICATIONS

	*APPLN. NO.	*FILING DATE	*INVENTOR	CLASS	SUBCLASS	

## FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

## OTHER ART (including Author, Title, Date, Pertinent Pages, Publisher, Place of Publication, Etc.)

HFW	Rajesh Kumar et al., "Interconnect and Noise Immunity Design for the Pentium 4 Processor," Intel Technology Journal Q1, 2001; pp. 1-12 <i>No month given</i>					
HFW	Daniel Wiklund et al., "SoCBUS: Switched Network on Chip for Hard Real Time Embedded Systems," Eight Unnumbered Pages, Date No Earlier Than 2002 <i>APRIL 2003</i>					
HFW	Ismail et al., "Repeater Insertion in RLC Lines for Minimum Propagation Delay," 1999 IEEE, pp. VI-404-VI-407 <i>no month given</i>					
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HFW	Youngsoo Shin et al., "Coupling-Driven Bus Design for Low-Power Application-Specific Systems" DAC2001, June 18-22, 2001, Las Vegas, Nevada					
HFW	Mircea R. Stan, et al, "Bus-Invert Coding for Low-Power I/O," IEEE Transactions on Very Large Scale Integration (VLSI) systems, Vol. 3, No. 1, March 1995					
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EXAMINER

*Howard Williams*

DATE CONSIDERED

*14 April 2005*